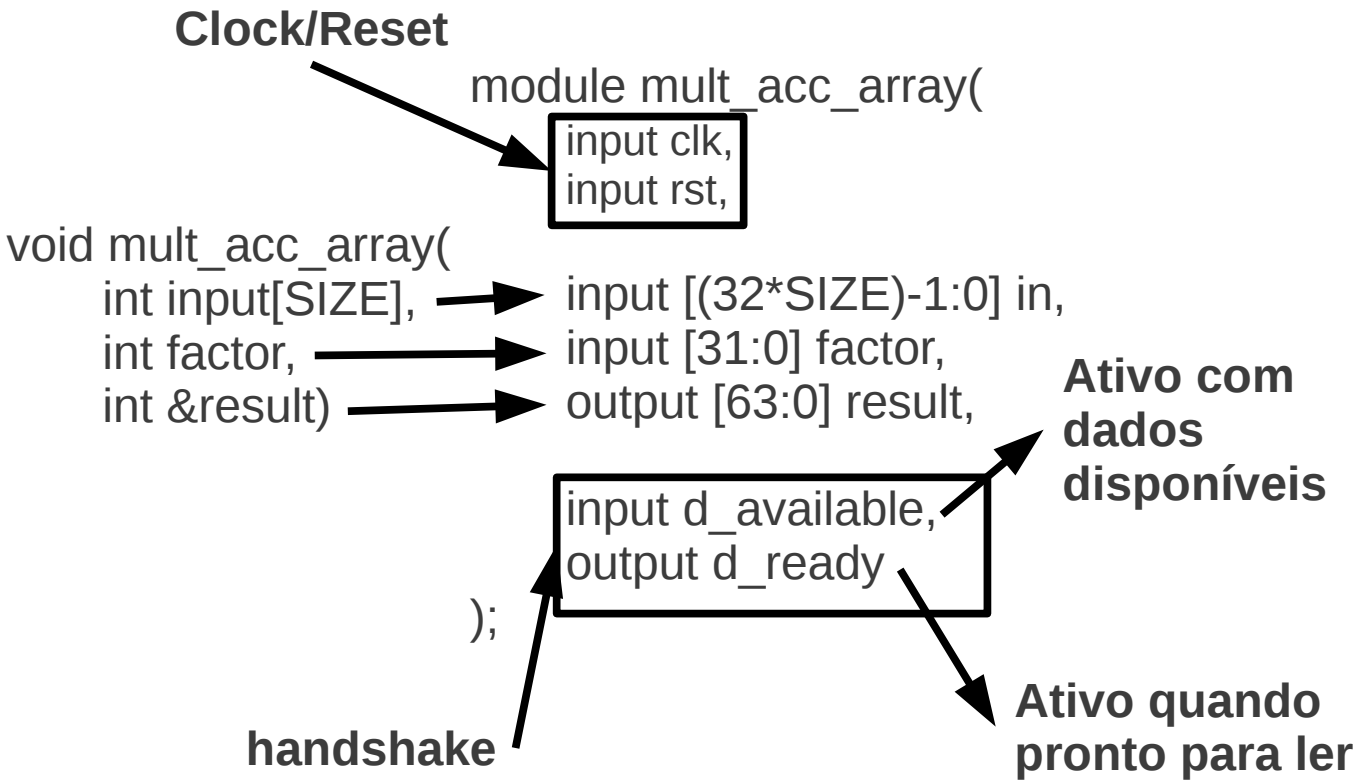
Clock/Reset
module mult_acc_array(
input clk,
input rst,
void mult_acc_array(
int input[SIZE],
int factor,
int &result)
input [(32*SIZE)-1:0] in,
input [31:0] factor,
output [63:0] result,
Ativo com dados disponíveis
input d_available,
output d_ready
);
handshake
Ativo quando pronto para ler