ForSyDe's embedded compiler

First development stage results.

Alfonso Acosta

alfonso.acosta@gmail.com

ICT/ECS Royal Institute of Technology, Stockholm

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Outline

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• Let's see a simple example. Design a serial adder using components in 5 simple steps.

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) Create a process function which adds one to its input

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2) Create a system function corresponding to the unit adder

addOneProc :: Signal Int -> Signal Int
addOneProc = mapSY "addOne" addOnef

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3) Subsystem definition associated to the unit adder

```
addOneSysDef :: SysDef (Signal Int -> Signal Int)
addOneSysDef = $(newSysDef 'addOneProc ["in1"] ["out1"])
```

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4) Create the main system function

addFour	:: Signal Int -> Signal Int	
addFour	<pre>= \$(instantiate "addOne3" 'addOneSysDef)</pre>	•
	<pre>\$(instantiate "addOne2" 'addOneSysDef)</pre>	
	<pre>\$(instantiate "addOne1" 'addOneSysDef)</pre>	
	<pre>\$(instantiate "addOne0" 'addOneSysDef)</pre>	

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5) Finally, build the main system definition

addFourSys :: SysDef (Signal Int -> Signal Int)
addFourSys = \$(newSysDef 'addFour ["in1"] ["out1"])

Design Flow Using Components

figures/compflow

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Supporting any Signal type

- Challenge: support simulating signals of any type.
- How is it possible? Typeable and Lift constraints.

```
class Typeable a where
  typeOf :: a -> TypeRep
toDyn :: Typeable a => a -> Dynamic
class Lift t where
  lift :: t -> Q Exp
```

```
delaySY :: (Typeable a, Lift a) =>
ProcId -> a -> Signal a -> Signal a
```

- What about the instantiation boilerplate code?
 - GHC supports automatic derivation of Typeable
 - I Improved Igloo's Lift library (GHC 6.10 won't need it, i.e. instance Data a => Lift a will probably be included).

data LogicVal = High | Low deriving (Eq, Typeable)
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A new sequential simulation backend has been implemented



- It detects combinational loops (i.e. loops not including a delaySY process).
 - The detection was impossible with the previous stream-based signal implementation.
- Completely usable but still not optimal:
 - Due to some implementation problems, simulation is strict and its
 efficiency could be improved.

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- The Equalizer was ported to the new compiler API and is correctly simulated
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- Previously, ProcFuns had to be selfcontained.
 - i.e. The translation backends didn't have a way of accesing the external scope of a ProcFun, for instance:

 New functions allow to pass parameters without loosing encapsulation:

```
defArgVal :: (Lift a, Typeable a) => ProcFun (a -> b) -> a
-> ProcFun b
defArgPF :: ProcFun (a -> b) -> ProcFun a -> ProcFun b
```

Implementation of filterSY

filterSY id pred = mapSY id (filterer 'defArgPF' pred)

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- I got stuck finding workarounds for many of them.
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- VHDL backend
 - What primitives types to accept?
 - Custom types?
 - What Haskell subset in ProcFuns?
 - Process identifiers. Continue with current approach?

Bureaucratic issues

- Release
 - When should the package be released in Hackage?
 - What version number should it carry?
 - Name? ForSyDe vs ForSyDeStdLib
 - License, copyright holder, maintainer e-mail.
- Resources
 - Darcs repository
 - Mailing list archives

VHDL backend

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Bureaucratic issues

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Resources

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Outline

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- Finish the VHDL backend
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